Random events recorder

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Abstract

The architecture of the device recording randomly occurring events has been described in the present study. A/m device has been designed and built in order to enable the recording of broad – band acoustic emission signal (AE). The system of the recorder has been configured in the manner enabling its operation in the autonomous unit operation mode or its application as IBM PC extension card. The operation of the recorder is controlled by the internal MCS51 micro-controller. High speed ADC converter and associated statistic RAM memory are also incorporated. The system of the recording has been supplemented with the additional ADC converters and several I/O universal lines in order to enable the monitoring of slowly varying experiment parameters.

1. Introduction

Many various types of stresses are generated in a solid body in the course of its mechanical working or heat treatment. When critical threshold levels are exceeded or in the case of phase transformation, a part of stress energy can be emitted in the form of elastic waves package. The phenomenon consisting in generation and propagation of such a wave is defined as acoustic emission (AE) [1]. The acoustic emission waves are characterized by variable amplitude and frequency and occur in the manner similar to random occurrence. Their frequency spectrum is included in the range between 20kHz and 1MHz.

AE signal sampling with the frequency of at least 2MHz is required in order to enable computerized recording of wide – band of AE signal. However the recording of AE wave is quite a difficult task owing to random nature of AE phenomenon. Therefore a high speed computer with the sufficient RAM memory capacity is necessary. Owing to the limited RAM memory capacity, the measurement duration is also limited. Further limitation of recording time is also possible owing to random nature of the phenomenon under monitoring. In the case of continuous recording of random phenomenon, only some fragments

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of the obtained spectrum are interesting in view of potential analysis – remaining part of the spectrum should be rejected.

Another problem is associated with the attempt to select some interesting events occurring in the whole range of recorded AE waves spectrum. Any attempts of „manual searching" of data set are extremely arduous. Therefore only the use of special program enabling the execution of searching process and generation of a new file containing exclusively the data suitable for later analysis (and archiving) is recommended.

2. Assumptions

The system of the recorder to be combined with the IBM personal computer has been designed and built in the framework of the present study with consideration of the problems indicated above. The following assumptions have been made in the course of interface designing phase:

- the system operation will be possible in the form of extension card in the IBM personal computer or in the form of an autonomous unit to be controlled by means of IBM via serial transmission channel, RS232;
- maximum AE signal sampling frequency will be equal to 2MHz and the data obtained from measurement will be saved in the area of inner RAM memory of the recorder;
- the area of inner RAM memory with the measurement data will be accessible at any time – also in the course of the measurement;
- specialised analogue – and – digital detector system will enable making the decision regarding commencement and completion of AE signal recording, in respect of hardware;
- after commencement of the recording process, all information referring to the current recording conditions will be recorded except for AE signal measuring data;
- all settings of hardware incorporated in the recorder can be altered by means of the program installed in the IBM personal computer and operating WIN95/98 environment.
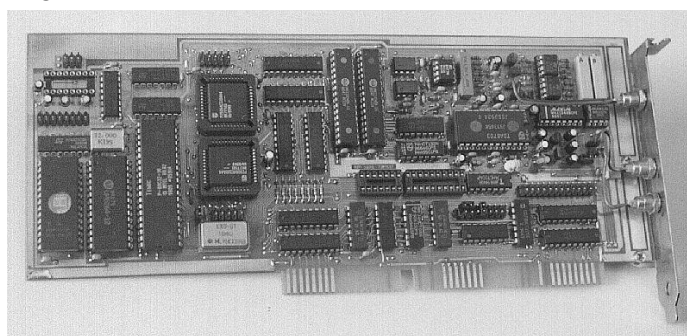

Photo. 1. Appearance of random events recorder

Refer to Photo No 1 for the illustration of random events recorder designed on the basis of the assumptions presented above. The recorder has been built as IBM PC extension card with standard EISA interface [2]. The card, when looking from the computer side, encompasses a single 16-bit I/O register. Any of the following addresses of the card can be set individually by means of jumpers: 240H, 260H, 280H, 300H, 320H or 340H. Any of three INT interrupt channels (5, 6 or 7) can be also assigned to the recorder card by means of jumpers.

2. Architecture of the recorder and measuring procedure

AE phenomenon consists in the series of random packages quickly varying voltage signals which should be recorded. The occurrence of waves package is called „the event". The ideal representation of such an event has been illustrated in Figure 1. The purpose of the random events recorder is to enable the recording of each recognizable event. For instance repeated exceeding of specified voltage threshold by AE signal can be used as the criterion for commencement of logging. Such a status has been illustrated in Figure 1. The signal with the amplitude exceeding the established voltage threshold is amplified and transformed to obtain the binary form – pulses. After logging of a specified number of pulses, recording procedure can be commenced. Owing to delay of the recording commencement in relation to the event commencement time, a part of AE wave could be not recorded. Such part is called „history" in Figure 1.
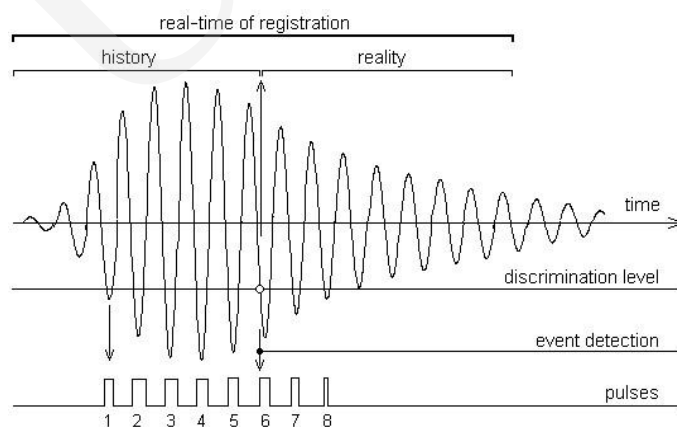

Fig. 1. Representation of hypothetical event to be recorded

In order to prevent any data loss, continuous measurement of AE signal amplitude has been assumed i.e. independent of a detected or not detected event. The data obtained from measurement will be saved in a separated and limited area of RAM memory forming a cyclical register. The new data are overwritten periodically under the specified address in a/m register. The interval

of overwriting is proportional to the scale of cyclic register. After detection of the event, the registration will be carried out within 50% of the size of cyclic register. Therefore the data accumulated before the detection of the event will not be cancelled and the reproduction of measurement „history" will be possible. After complete filling of RAM memory area being discussed, a new area of cyclic register should be indicated by the memory management system.

Refer to Figure 2 for the block diagram of random events recorder. The micro-controller µC (80C52) has been applied as the recorder operation managing element. An analogue electrical signal from the sinusoidal waves package (AE) is transmitted to the interface card via S input and supplied to the high speed analogue – digital converter F_ADC (TDA8703 [3]) and to D discriminators system. The signal amplitude is compared with the voltage threshold UDAC in the discriminators system. The voltages exceeding UDAC level are amplified and transformed into the digital form – pulses. The latter are supplied to the micro-controller system µC and to the timing system T in order to detect any potential events among the group of pulses. Parallel to the discrimination process being discussed, the analogue signal, after processing by means of high speed analogue – digital converter, F_ADC, is directed to X_RAM memory. ADC processing is carried out continuously. The address and the manner of measurement data saving in X_RAM are selected by means of Memory Management Circuit (MMC) controlled by means of two sources i.e. the events detector (T) and the micro-controller system (µC).
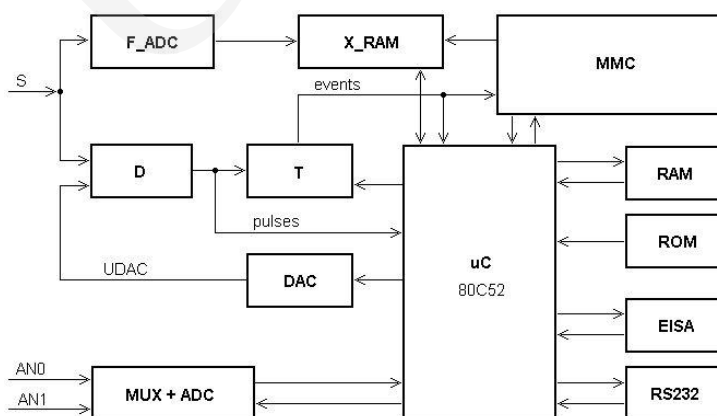

Fig. 2. Block diagram of random events recorder

The RAM and ROM memory shown in Figure 2 are standard units enabling 80C52 micro-controller operation in the microprocessor mode. MUX+ADC system has been designed as the dual channel ADC converter enabling additional monitoring of experiment environment. The units EISA and RS232

are standard channel designed for data exchange between the recorder and the experiment management computer.

3. X_RAM Memory Management

As already mentioned, X_RAM memory should be accessible for F_ADC converter and micro-controller at any time. The recording or reading of data under any address within the address space in X_RAM memory will be possible by means of the micro-controller. The records to the selected area of the memory to be made in the cyclic and continuous manner will be possible by means of ADC converter. Apparent conflict of interests in the present case has been resolved using the alternative access to X_RAM memory to be provided with timing frequency of the converter F_ADC.
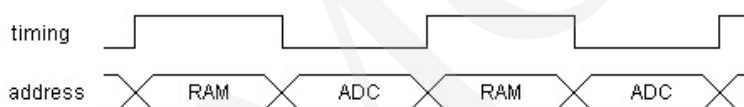

Fig. 3. Accessibility of X_RAM memory

The manner of memory access has been illustrated in a schematic manner in Figure 3. The complete address in X_RAM memory area has been defined under the names 'RAM address' and 'ADC address'. The device with memory access at a given moment is indicated by the timing signal. In the case of stabilized 'RAM address', the memory is accessible for the micro-controller – and in the other case the memory is accessible for F_ADC converter. All signals necessary for data recording or reading are prepared in the MMC system.

Refer to Figure 4 for schematic diagram of X_RAM memory management method by means of MMC system. The areas A, B and C called the areas of cyclic register have been determined in X_RAM memory area. Let us assume the area A is already occupied, the area B is an active working area and the area C has been not occupied yet. At any recording of data from F_ADC, the area of an active cyclic register and its inner address are indicated by the address in X_RAM memory generated by the MMC system. After any command of data record to working area, the inner address of cyclic register is increased by 1 in modulo(N) mode (N = size of the register). When X_RAM memory is accessible to the micro-controller system, the address indicated by the controller is defined by the MMC system to enable data recording or reading. The buffering in MMC system is provided for any information to be recorded or to be read from X_RAM memory in order to enable asynchronous cooperation of the micro-controller and X_RAM memory. The information regarding satisfactory completion of reading or recording process is transmitted to the micro-controller via INT interruptions. In the case of disabling of F_ADC converter, X_RAM

memory is directly accessible for the micro-controller, without using any INT interruptions.
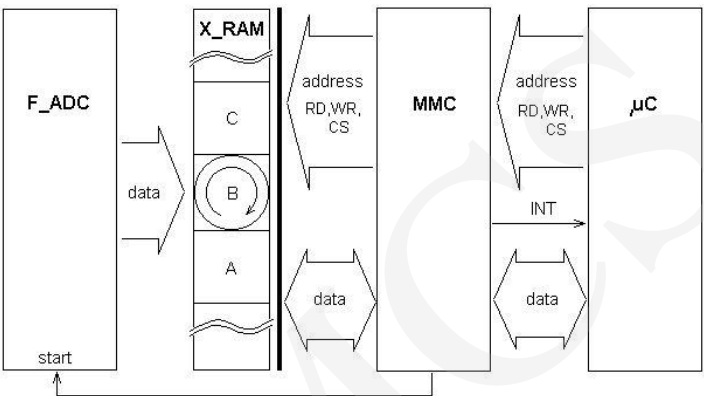

Fig. 4. Schematic diagram illustrating the manner of X_RAM memory management

The part of MMC system responsible for X_RAM memory access management has been illustrated in Figure 5. The system consists of adjustable timing signal generator C, two counters L1 and L2, two multiplexers MUX1 & MUX2 associated with address bus, the 1st multiplexer MUX3 of data bus and CB block designed for RD and WD signals generation for X_RAM memory. The data bus buffering registers designed for data exchange between X_RAM memory and micro-controller have been not indicated in the drawing. The count of L1 counter is changed in each cycle of F_CLK signal timing. The count of L2 counter is changed via EE line after each detection of AE event.
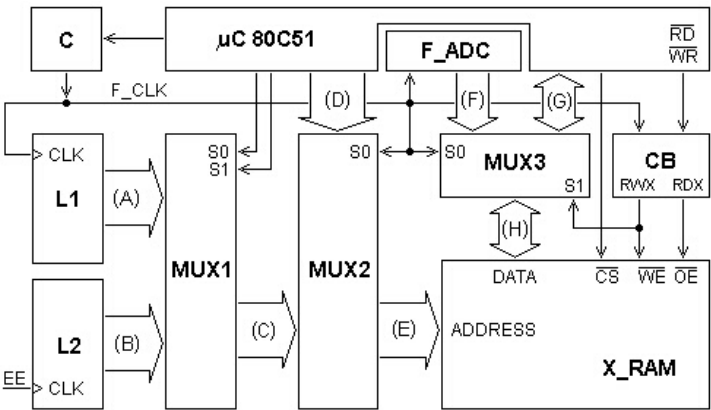

Fig. 5. Block diagram of memory management system

   Individual data buses and address buses in the drawing have been indicated by means of block letters from A through H.

   The rectangular clock signal F_CLK is generated by means of generator C controlled by means of the micro-controller. The signal is used for F_ADC converter timing and for assignment of the access to X_RAM memory (refer to Figure 3 for timing signal). The lines of address bus E, the lines of data buss H and control signals RDX and WRX are used for direct X_RAM memory control. The summary of address and data line is defined in MUX2 and MUX3 multiplexers in the form of logic status of F_CLK line.

Table 1. Diagram of connections of bus C and buses A and B

C bus	S0 and S1 setting			
	S0=0, S1=0	S0=1, S1=0	S0=0, S1=1	S0=1, S1=1
C0	A0	A0	A0	A0
…	…	…	…	…
C7	A7	A7	A7	A7
C8	B0	A8	A8	A8
C9	B1	B0	A9	A9
C10	B2	B1	B0	A10
C11	B3	B2	B1	B0
C12	B4	B3	B2	B1
…	…	…	…	…
C(N)	B(N-9)	B(N-9)	B(N-10)	B(N-11)

   In the case of X_RAM memory connected to the micro-controller, the lines E and H are connected with the corresponding lines i.e. D and G in respect of functioning. In the case of X_RAM memory connected to F_ADC, the address bus E is connected to the bus C and data bus H is connected to the bus F. RDX and RWX signals used for X_RAM memory control, are generated in CB block and depend directly on logic status on F_CLK lines and on WR and RD line of the micro-controller.

   Owing to the manner of releasing, the lines of A bus indicate the inner address of cyclic register. The lines of B bus indicate the address of an active cyclic register. C bus consists of the elements being the components of A and B buses. The manner of construction is determined by the micro-controller using the controlling lines S0 and S1. The size of cyclic register is defined by the user changing the logic values of S0 and S1. The status of the lines S0 and S1 is determined before the measurement and maintained in the course of the measurement. Refer to Table 1 for the scheme of inner connections of MUX1 multiplexer for various logic values of S0 and S1 lines.

4. Software

The software for random events generator consists of BIOS program for the micro-controller and of user program installed in the recorder operation managing computer. BIOS program encompasses all procedures enabling complete configuration of the recorder and execution of the measurement as well as an interpreter of the commands being supplied to the recorder by means of RS232 or EISA channel.

Fig. 6. Graphical interface for the recorder operation supervising program

The user program has been prepared for operation in WIN_95/98 environment. The graphical interface of the program has been illustrated in Figure 6. The purpose of interface check boxes is to enable the determination of measurement parameters. The purpose of "card" menu box is to enable the configuration of the recorder in the managing computer system. The purpose of "files" menu box is to enable the recording of data obtained from measurement and the recording of measurement settings and their reproduction.

6. Summary

The random events recorder has been designed on the basis of assumptions presented in Item 2, as the device recording AE events represented by the electric signals sinusoidal waves packages. Owing to high natural frequencies of the waves, 20kHz-1MHz, the recorder system is suitable for the measurements with the sampling frequency included in the range between 250kHz and 2MHz with resolution of 8 bits. In order to detect the fact of occurrence of AE signals with essential importance for the experiment, the inner detection system consisting of discriminators with the adjustable voltage threshold has been

incorporated in the recorder. The elements of sinusoidal wave with the amplitude exceeding threshold value are converted into the digital form and generate so called "pulses" in the case of single exceeding of the threshold value and "events" in the case of multiple exceeding. The purpose of the detector is to enable the detection in a simple and differential mode. In the case of simple mode, the pulses are generated when the discrimination barrier is exceeded (Figure 1). In the multiple mode, the pulses are detected for positive and negative values of the amplitude of the signal being examined.

The recorder has been provided with a special time detection system with adjustable value of dead time to be used for selection of elements from the group of pulses, being attributable to the events. The purpose of the additional counting limit detection system is to indicate the events – discriminated events from among all selected cases. The number of pulses and the number of events occurring in the 'time box' established by the user is saved by the recorder. The discriminated events are recorded in the cyclic registers of X_RAM memory. The size of cyclic register e.g. 256, 512, 1024 or 2048 bytes is defined by the user. The whole size of X_RAM memory to be used for saving of information on random events amounts 128kB. The recorder has been supplemented by the additional memory block of 128kB to be used for acquisition of data referring to the number of pulses and the number of events in the course of "time box" to be used for recording of additional data required for the analysis of obtained measurement results e.g. starting addresses for individual cyclic registers and occurrence time of the events elapsed from the measurement commencement.

The digital system of events recorder and all elements of memory management circuit MMC have been built on the basis of 2 programmable logic systems XPLA from CoolRunner series [4].

At the moment, many universal types of DAQ modules with excellent technical parameters are offered by computer market [5,6,7,8]. For instance ADLINK PCI-9112 (9118, 9812) [5], NI PCI-6251 [6], DaqBoard 3000 (3001÷3006) [7], OME-A-822PGL (822PGH, 826PG) [8] universal cards with PCI or EISA interface or many others can be used for AE signal recording. The measuring system based on universal cards should be supplemented with the detector time of measurement commencement and the detector of occurrence of individual events to be recorded. The measuring system must be integrated with RTC timing system enabling precise time determination for the occurrence of individual events.

The structure of recorder card described in the present publication encompasses all required hardware components enabling AE signal recording in accordance with the assumptions included in Item 2. As mentioned above, the card incorporates the two data exchange channels: EISA and RS232 interfaces. RS232 interface enables the individual card operation i.e. out of the structure IBM PC. RS⇔USB converter enables the coupling of the recorder with the

standard computer via USB channel. EISA interface, actually becoming obsolete can be easily replaced by PCI interface built on the basis of easily available PCI bridges (e.g. PCI9050) [9,10].

Owing to the integrated circuits, used in the recorder, it is possible to in crease the sampling frequency up to 40MHz. Owing to possibility of re-programming of XPLA and BIOS structures of inner microprocessor controller, potential adaptation of the recorder for other measuring tasks is relatively simple.

The project was sponsored by a private enterprise i.e. FORTEST, Przedsiębiorstwo Innowacyjno-Wdrożeniowe s.c. Lublin.

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